REMARKS

This response is intended as a complete response to the Final Office Action dated November 2, 2005. In view of the following discussion, the Applicants believe that all claims are in allowable form.

CLAIM REJECTIONS

A. 35 U.S.C. §103(a) Claims 1-13, 15, 17-23, 29-30 and 32

Claims 1-13, 15, 17-23, 29-30 and 32 stand rejected as being unpatentable over U.S. Patent No. 6,620,631 issued September 16, 2003 to *Tao, et al.* (hereinafter *Tao*) in view of *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986) (hereinafter *Wolf I*). The Applicants respectfully disagree.

Independent claims 1 and 12 recite limitations not taught or suggested by any combination of the cited references. The Examiner has split the claim elements into distinct subcomponents and has attempted to apply the cited references to each subcomponent in order to reject the claims. However, the Applicants submit that this is not a proper rejection because the cited references do not teach or suggest that which is claimed as a whole. It has long been established that claims cannot be used as a template or framework from which to pick and choose among individual references to recreate the claimed invention, as the Examiner attempts to do in this instance.

The Examiner admits that *Tao* fails to teach or suggest adjusting a process recipe for an overetch step of the etch process using results of measuring the dimensions, as recited in claim 1, and adjusting a process recipe for an overetch step of the etch process of etching a layer of the film stack using results of measuring the dimensions, as recited in claim 12. (*Final Office Action*, p. 2, para. 4.)

The Examiner contends, however, that *Wolf I* teaches that an additional overetch step may be required in certain circumstances for complete removal of an etched film, and that it would have been obvious to use an overetch step in the process of *Tao*. However, even assuming *arguendo* that the Examiner is correct, such a combination of *Tao* and *Wolf I* would produce a process where an initial etch process may be modified

as taught by *Tao* and an overetch step may be additionally performed, if required, as suggested by *Wolf I*. As such, the addition of an overetch step to the process of *Tao* still fails to yield an etch process including the steps of adjusting a process recipe for an overetch step of the etch process using results of measuring the dimensions, as recited in claim 1, and adjusting a process recipe for an overetch step of the etch process of etching a layer of the film stack using results of measuring the dimensions, as recited in claim 12. Therefore, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield the limitations recited in either of claims 1 and 12.

Thus, the Applicants submit that independent claims 1 and 12, and claims 2-11, 29-30, 32 and 13, 15, 17-23 respectively depending therefrom, are patentable over *Tao* in view of *Wolf I*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

B. 35 U.S.C. §103(a) Claim 14

Claim 14 stands rejected as being unpatentable over *Tao* in view of *Wolf I* in further view of Silicon Processing for the VLSI Era, Vol. 4, by Wolf, Lattice Press (2002) (hereinafter *Wolf IV*) and Solid State Electronic Devices by Streetman, Prentice Hall (1990) (hereinafter *Streetman*). The Applicants respectfully disagree.

Independent claim 12, from which claim 14 depends, recites limitations not taught or suggested by any combination of the cited art. The patentability of claim 12 over *Tao and Wolf I* has been discussed above in Section A. *Wolf IV* and *Streetman* have been discussed earlier in the prosecution history (in Applicants' September 1, 2005 Response) as teaching refractory silicides and high-k dielectrics used as gate electrode materials and gate dielectrics and gate dielectrics formed from SiO_2 respectively. However, *Wolf IV* and *Streetman* fail to teach or suggest an etch method comprising the step of adjusting a process recipe for an overetch step of an etch process that etches a layer of a film stack using the results of measuring dimensions, as recited in claim 12. As such, the teachings of *Wolf IV* and *Streetman* may not be

utilized to modify the method of *Tao*, alone or in combination with *Wolf I*, in a manner that yields the limitations recited in claim 12. As such, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield all of the limitations recited in claim 12, from which claim 14 depends.

Thus, the Applicants submit that claim 14 is patentable over *Tao* in view *Wolf*, in further view of *Wolf IV* and *Streetman*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

C. 35 U.S.C. §103(a) Claim 16

Claim 16 stands rejected as being unpatentable over *Tao* in view of *Wolf I* and in further view of United States Patent No. 5,858,847 issued Jan. 12, 1999 to *Zhou et al.* (hereinafter *Zhou*). The Applicants respectfully disagree.

Independent claim 12, from which claim 16 depends, recites limitations not taught or suggested by any combination of the cited references. The patentability of claim 12 over *Tao and Wolf I* has been discussed above in Section A. *Zhou* has been discussed earlier in the prosecution history (in Applicants' September 1, 2005 Response) as teaching a method of fabricating a drain structure of a field effect transistor that uses a hard mask formed from SiON, SiO_2, or Si_3N_4. However, *Zhou* fails to teach or suggest an etch method comprising the step of adjusting a process recipe for an overetch step of an etch process that etches a layer of a film stack using results of measuring dimensions as recited in claim 12. As such, the teachings of *Zhou* may not be utilized to modify the method of *Tao*, alone or in combination with *Wolf I*, in a manner that yields the limitations recited in claim 12. As such, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield all of the limitations recited in claim 12, from which claim 16 depends.

Thus, the Applicants submit that claim 16 is patentable over *Tao* in view *Wolf I* and *Zhou*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

D. 35 U.S.C. §103(a) Claims 31 and 33

Claims 31 and 33 stand rejected as being unpatentable over *Tao* in view of *Wolf I* and further in view of Materials Science and Engineering by Callister, 4th Ed., John Wiley & Sons (1997) (hereinafter *Callister)*. The Applicants respectfully disagree.

Independent claims 1 and 12, from which claims 31 and 33 respectively depend, recite limitations not taught or suggested by any combination of the cited references. The patentability of claims 1 and 12 over *Tao and Wolf I* has been discussed above in Section A. *Callister* teaches that measuring instruments produce scatter or data variability; thus, an average value of collected data is commonly taken. However, *Callister* fails to teach or suggest an etch method comprising the step of adjusting a process recipe for an overetch step of the etch process using results of measuring the dimensions, as recited in Claim 1, or the step of adjusting a process recipe for an overetch step of the etch process of etching a layer of the film stack using results of measuring the dimensions, as recited in Claim 12. As such, the teachings of *Callister* may not be utilized to modify the method of *Tao*, alone or in combination with *Wolf I*, in a manner that yields the limitations recited in either of claims 1 or 12. As such, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield all of the limitations recited in claims 1 and 12, from which claims 31 and 33 depend.

Thus, the Applicants submit that claims 31 and 33 are patentable over *Tao* in view *Wolf I*, and further in view of *Callister*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

12/12/05

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